

Nanotube-based data storage devices

We examine designs and operational characteristics of a candidate for universal memory: carbon-nanotube-based electromechanical data storage devices. Memory cells based on the bending of cantilever and suspended carbon nanotubes, and the relative motion of the walls of carbon nanotubes are discussed. These devices show fast write and read speeds, high cell density, and allow nonvolatile operation.

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The rapid expansion of portable consumer electronics has created a demand for new designs of data storage devices with improved performance characteristics. Currently, there are three commercially available families of memory: dynamic random access memory (DRAM), static random access memory (SRAM), and Flash memory, which requires no power to store data. Consumer products typically use combinations of these three memory families, each having their unique advantages: DRAM is cheap, SRAM is fast, and Flash is nonvolatile. In the semiconductor industry, increasing miniaturization is beginning to place strains on existing technologies for data storage and computer memory, which could soon reach fundamental physical limitations. At the same time, rapid growth in mobile devices is creating a need to develop new memory technologies that can deliver low power operation and low standby battery drain. These trends have accelerated development efforts in universal memory products that integrate the best features of existing memory types into a single package and eliminate the growing technical challenges. A new universal memory chip should be cheap and compact, draw and dissipate little power, and switch in nanoseconds.

There are several possible candidates for universal memory that are being actively explored by the industry. The technologies that have already found a niche in the memory market include magnetoresistive RAM (MRAM), ferroelectric RAM (FRAM), phase-change memory (PRAM), and a number of other technologies are attempting to compete in nonvolatility with Flash memory and in speed and density with conventional SRAM and DRAM.

In this article, an insight is given into a new approach to storing memory bits that is based on carbon nanotubes (CNTs). It employs a simple electromechanical switching rule, according to which the device is held together by a balance of three major forces: electrostatic, elastostatic, and van der Waals. Technically elegant and innovative designs of CNT-based electromechanical data storage devices exploit CNTs as both molecular device elements and molecular wires for the read-write scheme. This is an emerging area in the universal memory market, in which only the fabrication of the first integrated working prototypes and single demonstrations of electromechanical devices for storing, reading, and writing information has been achieved so far¹⁻⁷. However, CNTs hold great promise for future bottom-up approaches to the manufacture of electromechanical memory devices, as the

exceptional properties and well-characterized structures of CNTs allow for very high density memories and strong resilience of devices to fatigue and breakage.

Data storage based on cantilever carbon nanotubes

A three-terminal memory cell based on cantilever CNTs⁸ is shown in Fig. 1. A conducting movable component, which could be a single- or multiwalled CNT, is connected to a source electrode and suspended above a stepped Si substrate containing drain and gate electrodes.

In a nonconducting state '0' (Fig. 1a), the nanotube is not in contact with the drain electrode. When a voltage is applied between the source and the gate electrodes, charge is induced in the cantilever nanotube and it is deflected towards the substrate. At a certain, so-called 'pull-in voltage', the nanotube comes into electric contact with the drain electrode. The device is now in a conducting state '1' (Fig. 1b). If the device remains stable in state '1' after the voltage is turned off, it can be used as a nonvolatile memory cell. In such a nonvolatile device, an additional 'pull-out voltage' pulse is required to return it back to the '0' state. The voltage applied to the drain electrode is typically small, < 1 V, and does not affect the value of the pull-in voltage. It is used to control the current between the source and the drain electrodes.

The first prototypes of a three-terminal cantilever memory cell have been fabricated using Au electrodes and multiwalled CNTs¹. In this device (Fig. 1c), multiple switching cycles have been achieved with the gate voltage ranging between 6 V and 20 V. The source–gate voltage–current characteristics have been measured in air at room temperature, demonstrating the suitability of CNTs for the development of data storage devices.

The operational characteristics of cantilever memory cells have been studied using continuum models based on linear and nonlinear beam theories, molecular dynamics, and combined molecular dynamics/continuum approaches^{9–12}. It has been shown that van der Waals forces have a substantial effect on the performance of cantilever memory cells and introduce some design constraints^{8,10}. Devices with small diameter nanotubes have stiction and adhesion problems, i.e. a CNT, when in contact with the metal electrode, adheres to the surface with a high binding energy compared with the nanotube's elastic energy. The effects are more profound for longer nanotubes positioned closer to the substrate⁹.

Numerical simulations¹⁰ reveal a significant difference in the write time for the '1→0' transition (0.02 ns) and the '0→1' transition (0.8 ns). In the '0→1' transition, although the nanotube bends quickly towards the drain electrode, it tends to bounce off the surface many times before coming to rest in position '1'. When the nanotube bounces, dissipative surface processes arising from phonon excitation in the drain electrode reduce the '0→1' transition time by two orders of magnitude¹⁰.

Three-terminal memory cells have also been fabricated using vertically aligned multiwalled CNTs grown in a controlled manner from the pre-patterned catalyst dots on the device electrodes^{3,4} (Fig. 2). This novel approach can not only be made compatible with existing Si technology, but also allows a dramatic increase in integration densities compared with conventional memory devices.

In the design⁴, the source electrode is electrically connected to earth ground. When the drain and gate electrodes are connected to a positive voltage supply, positive electrostatic charges build up in these electrodes, and negative charges build up in the source electrode. This

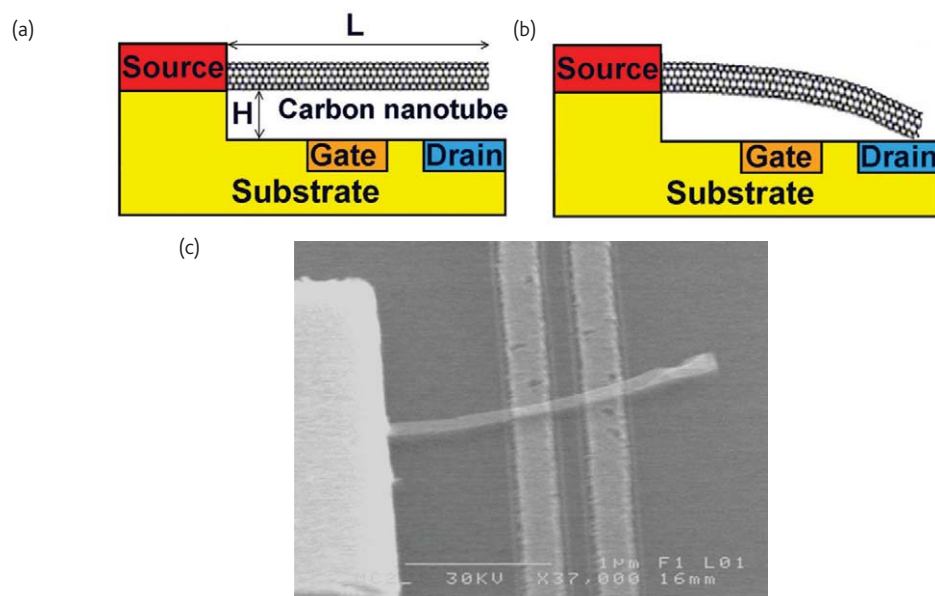


Fig. 1 A three-terminal memory cell based on cantilever carbon nanotubes: (a) nonconducting state '0', (b) conducting state '1', and (c) scanning electron microscope (SEM) image. (Reprinted with permission from¹. © 2004 American Chemical Society.)

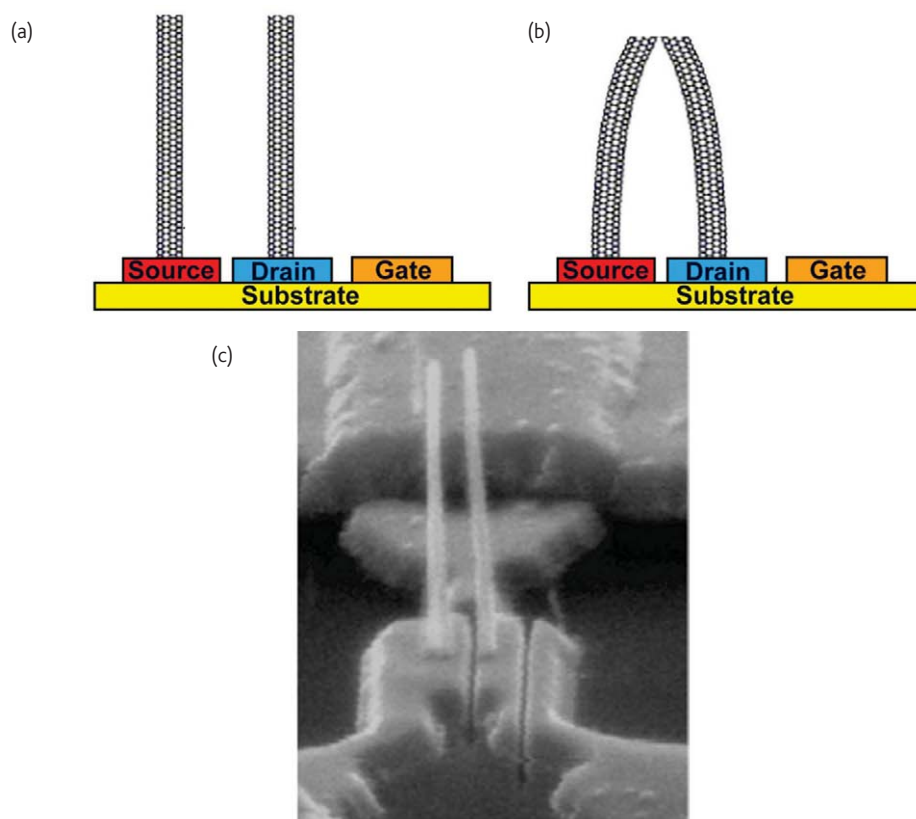


Fig. 2 A three-terminal memory cell based on vertically aligned multiwalled carbon nanotubes: (a) nonconducting state '0', (b) conducting state '1', and (c) SEM image. (Reprinted with permission from⁴. © 2005 American Institute of Physics.)

leads to electrostatic repulsion, pushing the CNT at the drain electrode away from the gate electrode and towards the CNT at the source electrode. When the pull-in voltage is applied, the source and drain electrodes make electrical contact, establishing the state '1' of the device (Fig. 2b).

It has been shown that once the voltage applied to the gate electrode is turned off, the source and drain electrodes can either remain held together in state '1' (typically for long nanotubes of $\sim 2 \mu\text{m}$ in length, for which the attractive van der Waals force is larger than the restoring elastostatic force), or alternatively return to the state '0' shown in Fig. 2a (typically for shorter nanotubes of $1.4 \mu\text{m}$ in length and less). This allows the fabrication of two different types of memory device with either volatile or nonvolatile behavior.

Recently, the performance of memory cells with vertically aligned CNTs has been significantly improved by making a CNT–insulator–metal (CIM) capacitor on the source¹³. A CNT grown from the source electrode is coated with a dielectric layer of SiN_x and a metal layer of Cr to form a CIM structure similar to the capacitors used in conventional high-density DRAM¹⁴. The CNT grown on the drain electrode is the mechanical element of the cell that, under electrostatic forces, bends and makes contact with the CIM capacitor. The CNT always snaps back after making contact and charging the

outer electrode of the CIM capacitor in a write or read operation. A logic '1' ('0') is flagged by charge (no charge) on the outer electrode of the capacitor, not by the physical contact. Replacing the SiN_x layer with high dielectric constant materials, such as Ta_2O_5 or SrTiO_3 would increase the capacitance and bias of the device to the level needed for gigabit-level applications ($\sim 10\text{--}15 \text{ fF}$ and $\sim 60\text{--}80 \text{ mV}$, respectively)¹⁴.

Data storage based on suspended carbon nanotubes

A new form of electromechanical memory based on suspended CNTs has been developed and manufactured by the start-up company Nantero, Inc. It is a high-density, nanotube-based nonvolatile random access memory (NRAMTM)^{2,15}.

In NRAM, a CNT bundle is suspended across a gap and connected to the source and drain electrodes. A metal gate electrode is positioned at the bottom of the gap underneath the suspended CNTs, so that charge can be induced in the CNTs by applying a voltage to the gate electrode. The applied voltage causes the nanotubes to flex and come into van der Waals contact with the gate electrode. This switches the device into the state '1' (Fig. 3b). The van der Waals forces make NRAM a nonvolatile device, as they hold the CNTs in the bent position until the pull-out voltage is applied to turn the device back to the '0' state (Fig. 3a). For nonvolatile conditions, the linear dimensions of the device

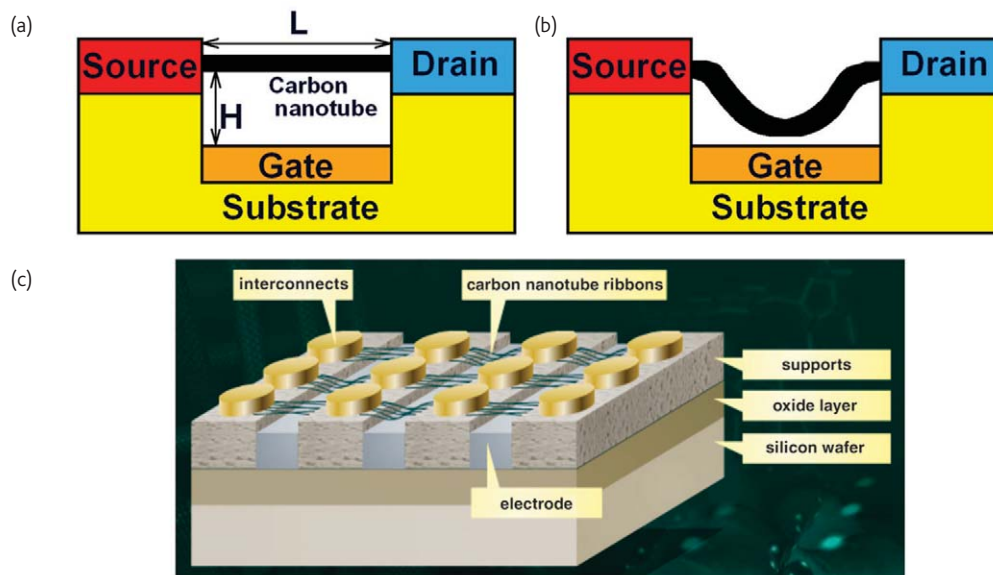


Fig. 3 A three-terminal memory cell based on suspended carbon nanotubes: (a) nonconducting state '0', (b) conducting state '1', and (c) Nantero's NRAM™. (Courtesy of Nantero, Inc.)

are carefully chosen so that the ratio of the length of the suspended nanotubes over the depth of the gap is kept equal to ten¹⁵.

The operational characteristics of NRAM have been modeled using molecular dynamics^{1,9}, continuum models^{1,16}, as well as other static and dynamic approaches¹⁷. One study⁹ suggested that the pull-in voltage of a memory cell based on suspended nanotubes is greater than that of a cell based on cantilever nanotubes with the same geometry, because CNTs fixed at both ends are stiffer and show smaller deflections. It also concluded that for a cell based on suspended nanotubes, the van der Waals interactions between the CNTs and the graphite gate were not significant. In the actual NRAM device, the van der Waals interaction between the CNTs and the oxide material of the gate electrode is a key parameter that defines the performance and nonvolatility of the device^{16,17}. The nonvolatility of NRAM could be improved by increasing the length of suspended CNTs, decreasing the gap between the CNTs and the gate, or by selecting a type of oxide layer that increases the van der Waals interaction effects. Stronger van der Waals interactions would lead to a decrease in the pull-in voltage, while the pull-out voltage is increased. Therefore, the pull-in and pull-out voltages should be carefully selected.

In NRAM, the tunneling resistance depends exponentially on the CNT deflection, invoking a sharp transition from the '0' to the '1' states when the voltage on the gate electrode is varied and the source–drain voltage is fixed^{16,17}. For a given structural geometry and a fixed low voltage on the gate electrode, the '0→1' transition time increases with larger diameters of the suspended nanotube, and, at a certain diameter, NRAM stops operating as a memory device. Similarly, the '0→1' transition time increases with the depth of the gap. The diameter of the suspended CNT is another parameter that can affect the nonvolatile behavior of NRAM^{16,17}. Other issues that

could potentially affect the operation of NRAM and its nonvolatility are temperature effects, such as thermal fluctuations of suspended nanotubes, and contact effects with the gate substrate.

Data storage based on telescoping carbon nanotubes

The achievement of the controlled and reversible telescopic extension of multiwalled CNTs¹⁸ led to a suggestion for a route towards an electromechanical switch based on CNT telescopic extension¹⁹. The telescoping process has been found to be fully reversible and has been repeated a number of times without apparent damage to the sliding surfaces¹⁸. Since then, the first nonvolatile device that operates using CNTs as low-friction bearings has been fabricated⁵.

This device consists of two open-ended multiwalled CNTs attached to the source and the drain electrodes (Fig. 4c). The CNTs are separated by a nanometer-scale gap with the gate electrode positioned between them. Switching occurs through the electrostatically initiated sliding of the inner core of a multiwalled CNT out of its sleeve. This closes the gap between the CNTs and establishes a conducting state '1'. The device has been shown to require <10 V of pull-in voltage on the drain electrode and <100 V of pull-out voltage on the gate electrode to produce robust and reversible '0→1' conductance cycles with extremely high switching speeds.

A number of further designs for data storage devices based on telescoping CNTs have been suggested that are based on double-walled CNTs with a short, capped inner wall acting as a shuttle^{20–23}. One of these is an all-carbon three-terminal memory cell²¹ with a single-walled CNT attached to the drain electrode and a CNT with a removed core attached to the gate electrode (Figs. 4a and 4b). The core of inner walls can be removed with the use of a nanomanipulator¹⁸.

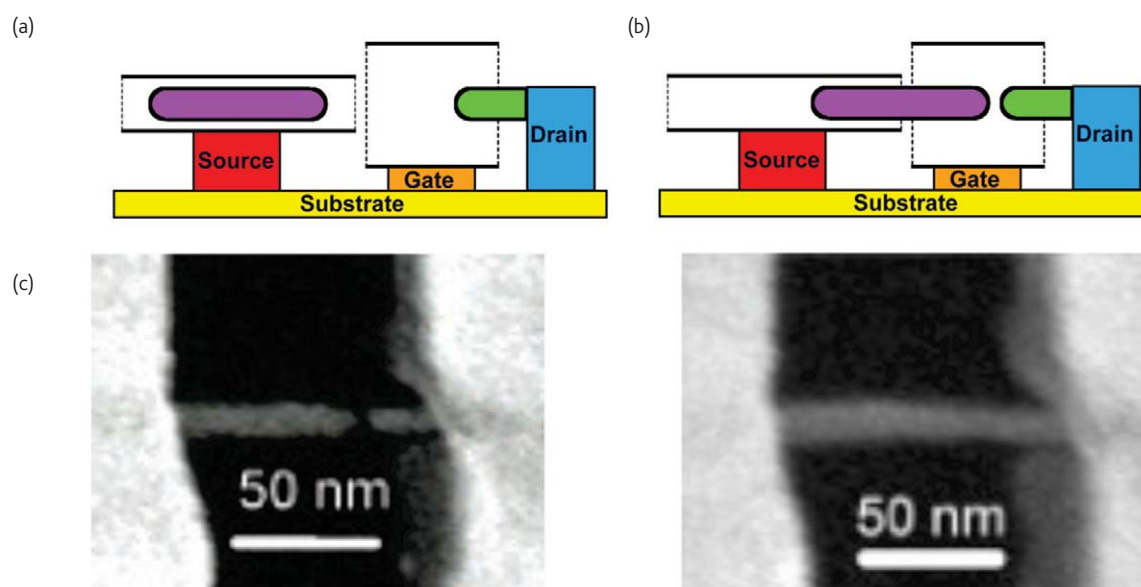


Fig. 4 A three-terminal memory cell based on telescoping carbon nanotubes. An all-carbon memory cell with a CNT attached to the gate electrode: (a) in nonconducting state '0', and (b) in conducting state '1'. (c) SEM images of a memory cell with a flat gate electrode. (Reprinted with permission from⁵. © 2006 American Chemical Society.)

The balance of the forces that defines the performance of the device has been analyzed²⁴. Electrostatic forces pull the shuttle out of the sleeve of a double-walled CNT attached to the source electrode, which comes into electric contact with the drain, thus establishing the connection (Fig. 4b).

After the power is switched off, the cell may remain held in state '1' by the van der Waals forces between the shuttle and the drain and the static friction force between the shuttle and the sleeve. This provides permanent contact and gives the nonvolatile capability of the device. At the same time, the capillary force of the weak van der Waals interaction between the walls of the double-walled CNT tends to retract the shuttle back into the sleeve, restoring the CNT to its original condition. When no voltage is applied, this force may provide a permanent gap between the CNT and the drain, keeping the cell in a nonconducting '0' state (Fig. 4a). Thus both nonvolatile and volatile behavior can be achieved in the device.

The all-carbon memory cell has some advantages in terms of future high-bandwidth applications, as CNT-made electrodes have much smaller dimensions compared with metal electrodes. Uniformity of all-carbon memory cell characteristics can be achieved by using identical switches made of CNTs with the same chirality indices. The volatility of the device is defined by the strength of the static friction force applied to the shuttle, which depends on the structure and the length of double-walled CNT. If the friction force is small, the device is stable in state '1' only if a voltage is applied, thus allowing the operation of a volatile memory cell. In a nonvolatile memory cell with all-carbon electrodes, as a result of thermal fluctuations of the components, the minimum size of the device at $T = 300$ K should be an order of magnitude greater than that at $T = 0$ K. To achieve optimal miniaturization and the highest operation frequencies, the device should be fabricated and used at very low temperatures. Under these conditions, the write density and switching frequencies will be

Table 1 Basic operational parameters of electromechanical data storage devices based on carbon nanotubes

Type of device	Linear size	Pull-in voltage, V	Operation frequency	Type of study
Based on cantilever CNTs	1–2.5 μm ^{1,4,7,13}	6–25 ^{1,4,7,13}	62–750 MHz ¹³	experiment
	30–2500 nm ^{8–10}	0.5–25 ^{8–10}	0.1–1 GHz ^{8,10}	theory
Based on suspended CNTs	800 nm–1.6 μm ^{1,6,25}	3.6–5 ^{1,2,6}	3–200 MHz ²⁵	experiment
	100 nm ¹⁷	0.3–3 ^{9,16,17}	33.3 MHz ¹⁷	theory
Based on telescoping CNTs	300 nm ⁵	4–10 ⁵	>1 GHz ⁵	experiment
	5–60 nm ^{20,21}	6 ^{20,21}	<100 GHz ²⁰	theory

Table 2 Performance characteristics of conventional and emerging memory technologies

Parameter	Conventional technologies			Emerging technologies			Prototypes
	SRAM	DRAM	Flash	MRAM	FRAM	PRAM	NRAM*
Read speed	fastest	medium	fast	fast	fast	fast	fast
Write speed	fastest	medium	slow	fast	medium	fast	fast
Programming voltage, V	N/A	N/A	high	low	medium	medium	low
Cell density	low	high	medium	medium/high	medium	high	high
Process technology, nm	130	80	56	130	130	90	22
Nonvolatility	no	no	yes	yes	yes	yes	yes
Future scalability	good	limited	limited	good	limited	excellent	scalable

*NRAM data should only be considered as a target established by Nantero, Inc.

significantly greater than those of memory cells based on cantilever and suspended nanotubes.

Basic parameters, such as operation frequencies, pull-in voltages, and size, of the three types of electromechanical data storage devices based on CNTs that have been considered here are given in [Table 1](#).


Conclusions and future challenges

The semiconductor industry is actively evaluating emerging memory technologies in the search of a new scalable technology. Although existing memory technologies continue to advance, providing faster, smaller, and cheaper memory, they are not expected to scale down beyond a very few additional process technology nodes.

The most widely used commercial nonvolatile memory – Flash – has a low write speed leading to slow random access. New memory technologies such as FRAM, MRAM, and PRAM are currently in use in a number of applications where the limitations of Flash are an issue. A comparison of the performance characteristics of conventional and novel advanced memory technologies is given in [Table 2](#), along with the first prototypes of CNT-based NRAM. These data show that

the new technologies present competitive capabilities and offer a number of advantages, notably fast random access and low power consumption.

Memory devices based on CNTs also have the potential to be advantageous allowing, at least in theory, densities higher than those of DRAM. The power needed to write to these devices is much lower than in DRAM, which has to build up charge on the plates. This means that CNT-based memory devices could not only compete with existing memories in terms of speed, but would also require much less power to run. Nantero, Inc. has recently demonstrated a prototype of a 22 nm NRAM switch and suggested that the NRAM switch will continue to scale down to below the 5 nm technology node.

All these advances, however, will become firm commercial reality only if radical changes in processing are found that gain precise control over the number and spatial location of CNTs over large areas. A production chip would require hundreds of millions of CNTs that are long enough to bend and have been manufactured cleanly and consistently. Additionally, new chemical processes will need to be proposed to align the CNTs better in the device, thus reducing the problem of reproducibility. 

REFERENCES

- Lee, S. W., et al., *Nano Lett.* (2004) **4**, 2027
- Rueckes, T., et al., *Science* (2000) **289**, 94
- Kim, P., and Lieber, C. M., *Science* (1999) **286**, 2148
- Jang, J. E., et al., *Appl. Phys. Lett.* (2005) **87**, 163114
- Deshpande, V. V., et al., *Nano Lett.* (2006) **6**, 1092
- Dujardin, E., et al., *Appl. Phys. Lett.* (2005) **87**, 193107
- Axelsson, S., et al., *New J. Phys.* (2005) **7**, 245
- Kinaret, J. M., et al., *Appl. Phys. Lett.* (2003) **82**, 1287
- Dequesnes, M., et al., *Nanotechnology* (2002) **13**, 120
- Jonsson, L. M., et al., *J. Appl. Phys.* (2004) **96**, 629
- Dequesnes, M., et al., *J. Eng. Mater. Technol.* (2004) **126**, 230
- Ke, C., et al., *J. Appl. Mech.* (2005) **72**, 726
- Jang, J. E., et al., *Nat. Nanotechnol.* (2008) **3**, 26
- Prince, B., *Semiconductor Memories*, 2nd Edition, Wiley, New York, 1996, Chapter 6
- Ward, J. W., et al., In: *Proceedings of the IEEE Non-Volatile Memory Technology Symposium*, 2004, 34
- Kang, J. W., et al., *Physica E* (2005) **28**, 273
- Kang, J. W., et al., *Physica E* (2006) **33**, 41
- Cummings, J., and Zettl, A., *Science* (2000) **289**, 602
- Forró, L., *Science* (2000) **289**, 560
- Maslov, L., *Nanotechnology* (2006) **17**, 2475
- Popov, A. M., et al., *Phys. Status Solidi A* (2007) **204**, 1911
- Bichoutskaia, E., *Philos. Trans. R. Soc. London, Ser. A* (2007) **365**, 2893
- Kang, J. W., and Jiang, Q., *Nanotechnology* (2007) **18**, 095705
- Bichoutskaia, E., et al., *Phys. Rev. B* (2006) **73**, 045435
- Sazonova, V., et al., *Nature* (2004) **431**, 284